

FIG. 4

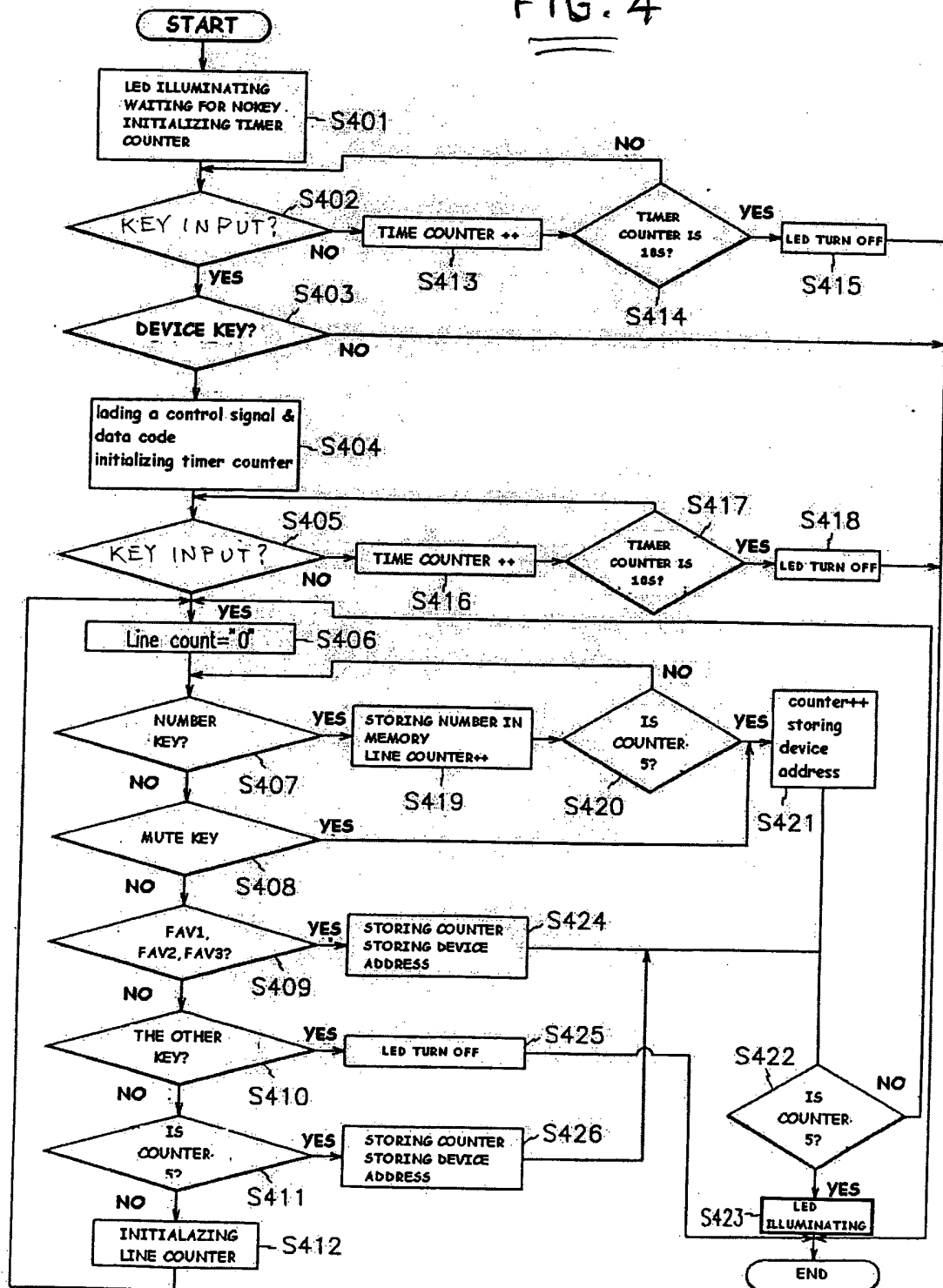


FIG. 5

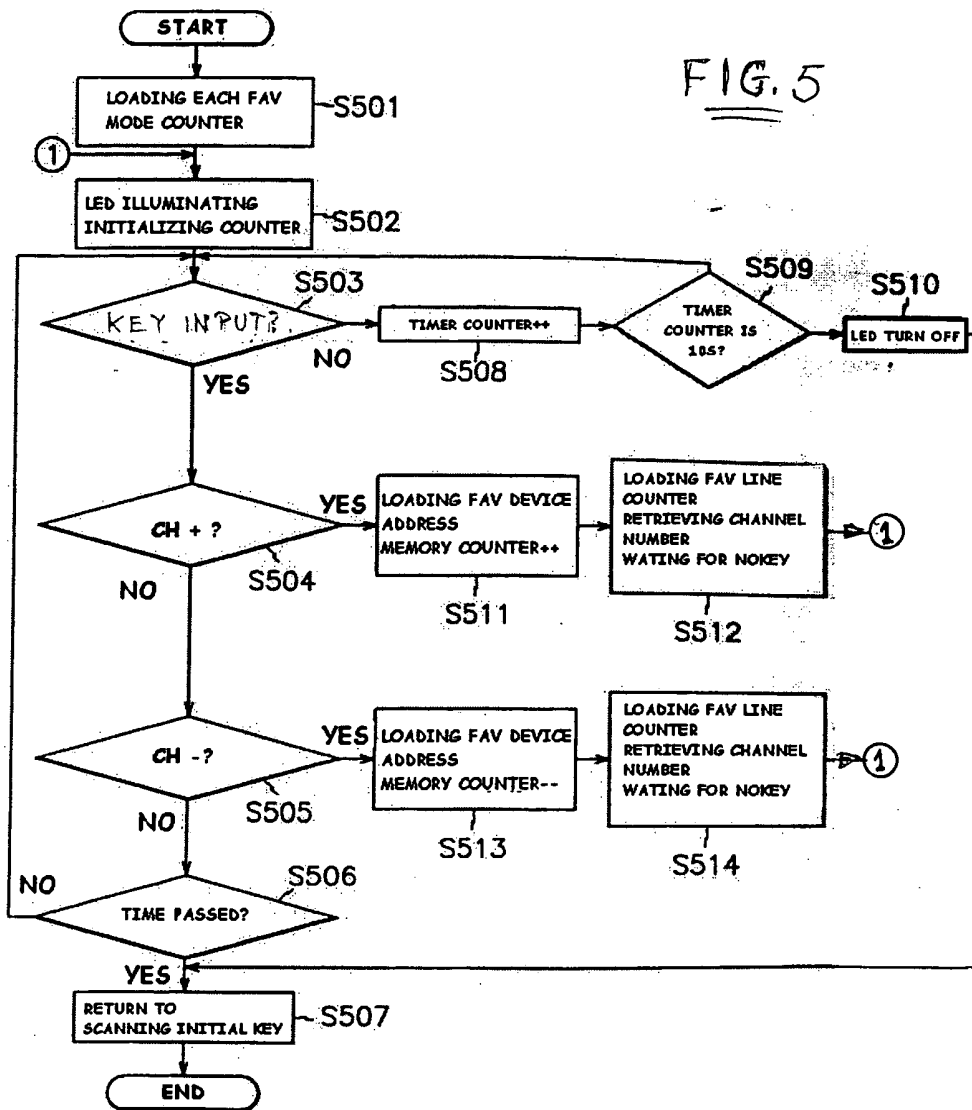


FIG. 2

| CH DN order | CH UP order | MEMORY COUNTER    |    |                |    | LINE COUNTER   |    |   |
|-------------|-------------|-------------------|----|----------------|----|----------------|----|---|
|             |             | M1                | 0  | 2              | 3  | ff             | ff | 3 |
|             |             | M2                | 1  | 2              | ff | ff             | ff | 2 |
|             |             | M3                | 1  | 2              | 3  | 4              | ff | 4 |
|             |             | M4                | 3  | 2              | ff | ff             | ff | 2 |
|             |             | M5                | ff | ff             | ff | ff             | ff | 0 |
|             |             | DATA REGION       |    |                |    |                |    |   |
|             |             | CONTROL REGION    |    |                |    |                |    |   |
|             |             | F1 Device address |    | F1 Max counter |    | F1 cur counter |    |   |

FIG. 3

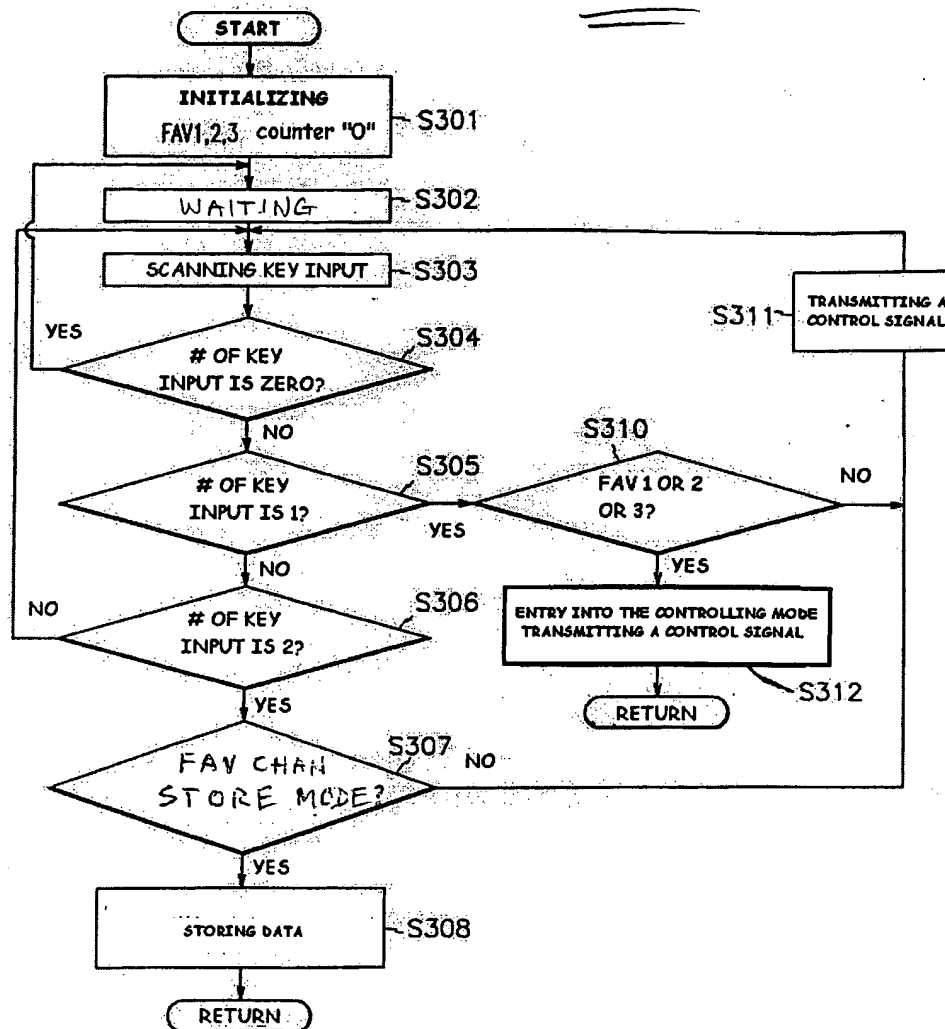


FIG. 1

